Holistic approach using accuracy of diffraction-based integrated metrology to improve on-product performance, reduce cycle time and cost at litho

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ABSTRACT

High-end semiconductor lithography requirements for CD, focus and overlay control drive the need for diffraction-based metrology[1,2,3,4] and integrated metrology[5]. In the advanced nodes, more complex lithography techniques (such as multiple patterning), use of multi-layer overlay measurements in process control, advanced device designs (such as advanced FinFET), as well as advanced materials (like hardmasks) are introduced. These pose new challenges for litho-metro cycle time, cost, process control and metrology accuracy. In this publication a holistic approach is taken to face these challenges via a novel target design, a brand new implementation of multi-layer overlay measurement capability in diffraction-based mode and integrated metrology.

Keywords: Overlay, integrated, in-line, on-product, diffraction, multi-layer, DBO, scatterometer, TMU, matching, metrology, accuracy, process robustness, matching to device, target design, productivity, track, MA time, HVM, cost.

1. INTRODUCTION

Both diffraction-based overlay (DBO) and integrated metrology (IM) are now successfully deployed in high-volume manufacturing (HVM) at 20nm node. DBO targets of size 16µm x 16 µm (known as YieldStar µDBO[7]) are used in production implementation. One of the most critical enablers in this deployment of µDBO has been the upfront prediction (well before a wafer measurement takes place) of overlay metrology accuracy via target design simulation software called "design for control" or D4C™. While traditional metrology indicators, such as precision ("TMU"), are of course important and good performances needs to be maintained, TMU is never used as the primary criteria for target and metro recipe selection for µDBO; instead significant attention is paid towards accuracy[1] as this has a direct impact to on-product performance and it is used for target and metro recipe selection in YieldStar µDBO. D4C is used to design all the overlay metrology targets for YieldStar. The measurement recipes are then carefully selected corresponding to the D4C target to ensure good accuracy, precision, speed and tool matching performance for all layers.

The implementation of IM is also complete and the benefit of IM in cycle time reduction is quantified.

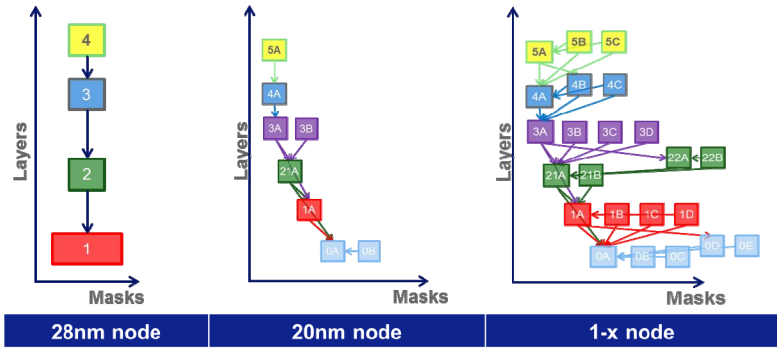

Figure 1. A typical schematic of a multi-patterning complexity in alignment and overlay

Going forward in 1-x development node, the number of immersion layers increases significantly which increases the burden on litho-metro cycle time. An additional challenge is the need for multi-layer overlay measurement in process correction (shown in figure 1). Multi-layer overlay requirements are mostly coming from the fact that a simple two-layer registration is no longer sufficient to optimize complex circuit design. An old example: the contact layer needs to be aligned to both active and poly within tight tolerances; since adjustments to overlay for these levels are not independent,

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it is essential to understand the relationship between all three layers[6]. Multi-patterning (figure 1) and process needs, such as via-last processes, add to the above needs for multi-layer overlay. Multi-layer overlay measurement requirements create a significant increase in litho-metro cycle time and cost (doubling or even tripling metro-sampling on many critical layers). In order to face this challenge of increasing litho-metro cycle time, "multi-layer μDBO targets" are introduced to enable multiple measurements in a single acquisition. This means the multi-layer combinations of overlay can be measured in a single acquisition (instead of separate acquisitions for each of the combinations) using a carefully designed single target. Such an implementation of multi-layer μDBO targets reduces the measurement time (enabling a double layer overlay in single acquisition means cutting down the MAM time by almost half for each layer-pair) and also effectively reducing already small real-estate of μDBO targets for each of the layer pairs.

Multi-layer μDBO targets are a must for IM to support measurements in a multi-layer situation. This is because the IM concept is fundamentally based on a single metrology tool per litho-cluster and does not entertain any increase in the number of metrology tools beyond one metrology tool per cluster (meaning the metro load necessary for APC must be supported by a single metro tool per cluster). This basically controls the CAPEX to be limited to one metrology tool per cluster. The use of IM (which is already proven for cycle time improvement in previous nodes) in conjunction with the use of multi-layer target delivers an effective solution necessary to control the increasing cycle time and cost driven by multi-layer overlay at 1-x node.

To further assist in the above concerns, faster "integrated" metrology systems in combination with fully automated track-logistics are deployed.

2. DEPLOYMENT OF DBO USING D4C TARGET DESIGN AND YIELDSTAR RECIPE SELECTION FOR ACCURACY

2.1 Common abbreviations used in the paper

μDBO is the diffraction-based overlay mode in YieldStar scatterometry[8,9,10,11,12] system capable to measure on-scribe as well as in-chip overlay.

TMU is Total Measurement Uncertainty (overall precision): $\mathrm{TMU} = \sqrt{(Dynamic\_precision)^2 + (\mathrm{TIS}_{\mathrm{mean}})^2 + (3\sigma_{\mathrm{TIS}})^2}$

Dynamic precision is reproducibility (3-sigma of multi-runs); TIS is Tool Induced Shift (a measure of the systematic error contribution to the overlay measurement resulting from the imperfection of the measurement system (tool-target optical interaction). Tool matching is separately evaluated (was not included in TMU) using a stringent specification.

Accuracy is matching to on-product overlay or device overlay. In absence of any better reference method to quantify accuracy, YieldStar μDBO measurement results are compared[1] with a specially designed overlay target that is made using product structure /pitch and can be measured at post etch step using a CDSEM. In this paper, overlay accuracy is defined by delta OVL (Mean+3sigma, full wafer) measured by YieldStar on μDBO targets (after develop) and CDSEM on device like targets (after etch). Note that the μDBO target pitches are different (larger) than the CDSEM targets have a much smaller pitch (similar to product geometry). Keeping in mind that the CDSEM measurements can be noisy at this level, the comparison to μDBO is done with a full wafer data (mean + 3 sigma of many points over the wafer).

2.2 Device-like performance using YieldStar overlay measurement on D4C targets

Goal of the product called "Design for control" or in short "D4C" is to generate and optimize metrology targets for the best on-product overlay performance. The design process includes a thorough simulation of various target designs for the "printability" of the target at production (litho) illumination condition. But having a printable target is not enough as the targets need to also generate the most optimum signal-to-noise on YieldStar (the metrology tool). Hence, the next step to printability is to simulate the target design for "detectability" on YieldStar sensor. The resulting top target designs (that are most printable in litho and provide the best signal-to-noise in YieldStar) go through a process robustness simulation. In this process robustness step, typical variations in the process stack are injected and the performances of each of these target designs are simulated. Only those target designs that can survive these process variations are selected. Next step is "device matching" simulation step. In this step only those target designs that mimic product behavior (have the same aberration sensitivity as product features) are selected.

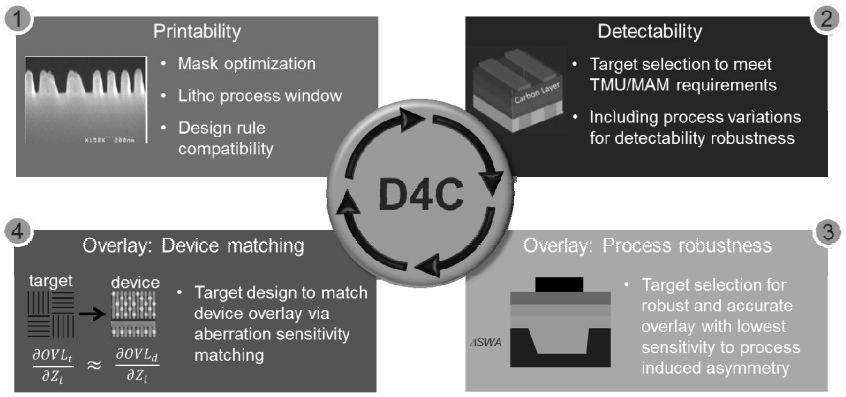


Figure 2. Design for control (D4C) optimizes targets for best on-product performance (overlay target design optimization concept for detectability and overlay accuracy)

The above steps are followed for every layer and targets are printed on wafer and measured by YieldStar. It is found that the YieldStar measurement data from the best target predicted by D4C matches well with CDSEM overlay measurements (where a specially designed overlay target that is made using product structure /pitch and can be measured at post etch step using a CDSEM). Below is an example of CDSEM overlay measurement on a FEOL layer (at after etch) and is compared to YieldStar measurement on a D4C generated target (at after develop). The above results are from the target located in location left-bottom circle of the figure below. Similar comparison is made for the other locations on the die to ensure a good comparison.

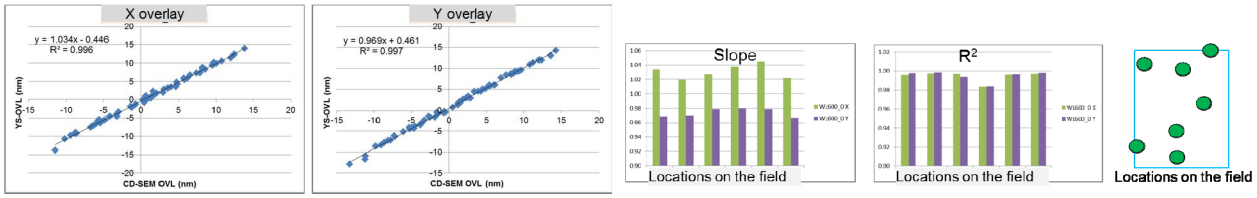


Figure 3. A FEOL layer measurement result comparison between YieldStar overlay measurement on a D4C generated target (after develop) to CDSEM measurement of overlay on a device like structure (after etch)

Additionally self-consistency (setting to setting, target to target) during YieldStar measurement is checked for accuracy and robustness (this does not require validation by CDSEM). In the example shown below, an accurately designed D4C target shows consistent results (overlay fingerprint) through multiple YieldStar recipes (different wavelengths, polarizations etc.).

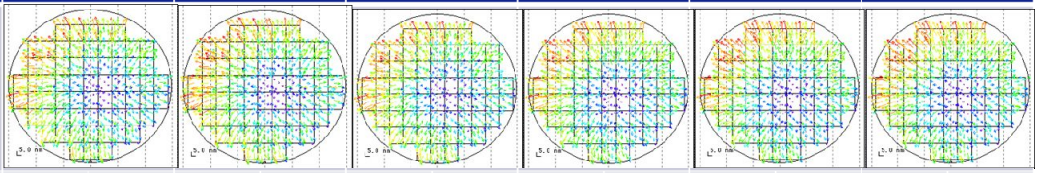
	Setting 1		Setting 2		Setting 3		Setting 4		Setting 5		Setting 6	
OVL												
	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
Wafer Exp.	0.048	0.057	0.051	0.058	0.049	0.058	0.050	0.056	0.050	0.057	0.050	0.056

Figure 4. Self-consistency of YieldStar setting-to-setting (measured on a D4C target) indicates measurement accuracy

Using these accurate target measurements, YieldStar is rolled out to HVM at 20nm node. A major parameter to track HVM capabilities of overlay measurement tool is tool to tool matching.

Results below show that 125 YieldStar tools running in production are meeting a matching spec of <10% of on-product-overlay requirements on 8 different production layers. For point-to-point matching, a production layer wafer is run on each of these 125 YieldStar tools and overlay measurement wafer map from 200 points on this wafer from each tool is

compared to overlay measurement from a single "golden" YieldStar tool. A point-to-point delta between overlay form the tool of interest (one of those 125 tools) and the golden tool is calculated for the full wafer. The maximum delta found among these 200 points is then calculated (in absolute number) as the point-to-point max delta and is expressed as a percentage of on-product overlay (OPO) requirements which is different for different product layers. This is plotted in the y-axis of the chart below. It can be seen that point to point max delta overlay between any YieldStar tool compare to the "golden" YieldStar always remain less than 10% of OPO.

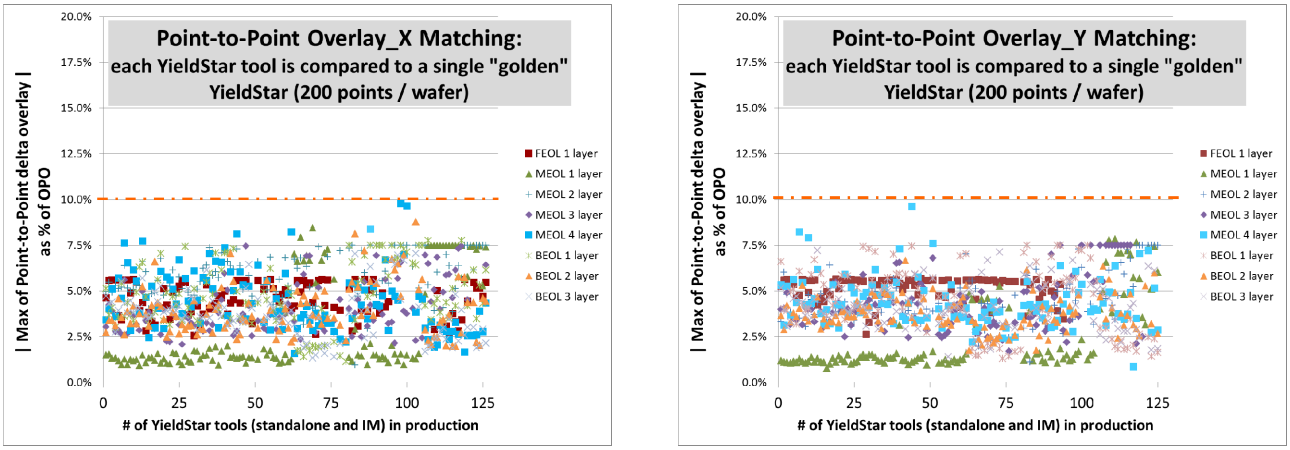


Figure 5. 125 YieldStar tools' overlay matching within 10% of OPO in HVM (on 8 production layers); Point-to-point matching using 200 points sampling / wafer

3. MULTI-LAYER OVERLAY REQUIREMENTS AND SOLUTION WITH D4C CREATED MULTI-LAYER µDBO TARGETS TO REDUCE METRO TIME & COST

Multi-layer overlay requirements are mostly coming from the fact that a simple two-layer registration is no longer sufficient to optimize complex circuit design. Moreover, multi-patterning and via-last processes add to the needs for multi-layer overlay. A simple calculation is shown in the chart below. Going from 20nm node to 1-x node the number of immersion layers go up by 50%; however, the actual number of overlay metrology steps go up by almost 100% driven by multi-layer measurement needs. This also increases the corresponding total metrology time at 1-x node by almost 80%. If nothing special is done, this will drive up the CAPEX needs for metrology tools at 1-x node.

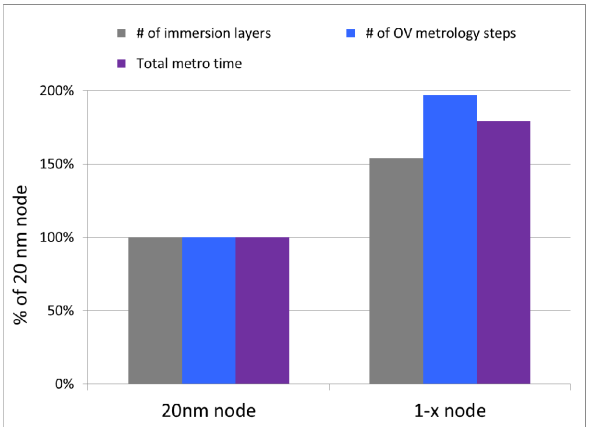


Figure 6. Significant increase in metrology load going to advanced nodes (Immersion layers)

In order to face this challenge in the increase of above mentioned cost and litho-metro cycle time (discussed in chapter 4), D4C generated "multi-layer µDBO targets" are introduced to enable multiple measurements in a single acquisition. This means majority of the multi-layer combinations of overlay can be run using a carefully designed single target where

multi-layer combinations can be measured using a single acquisition instead of separate acquisition for each of the combinations.

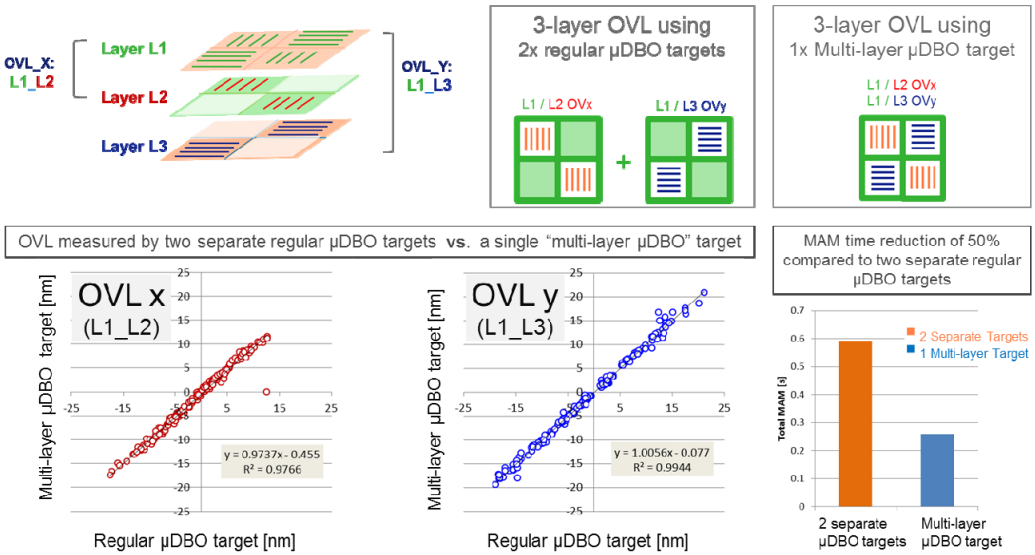


Figure 7. Multi-layer µDBO (combo) targets measuring overlay among 3 layers (1-x node FEOL layer)

The challenge of course is to be able to use a single acquisition setting for the both layer pair combinations. Here D4C helps significantly to design target pairs such that a single acquisition can be used.

With a proper implementation of the multi-layer target (as above), the impact of metro time increase mentioned in the previously discussed figure (figure 6) can be reduced significantly. Actually, the # of metro tools per immersion metro pass can be reduced by almost 40% with the implementation of multi-layer overlay measurements in single acquisition on YieldStar.

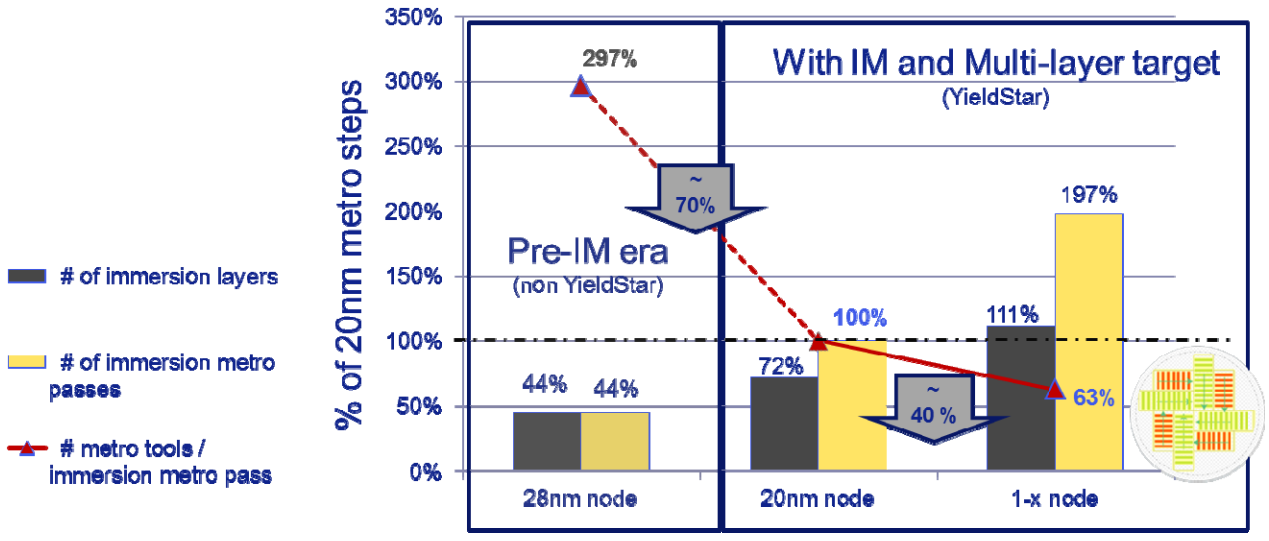


Figure 8. D4C generated multi-layer targets can reduce CAPEX by 40% in 1-x node immersion layers

4. INTEGRATED METROLOGY (IM) & TOTAL LITHO-METRO CYCLE TIME (CT)

Metrology time discussed in previous chapter is actually a small part of the total litho-metro cycle time. Measured data shows that transfer times from litho to metro (involved when standalone metrology is used) is actually much larger than the metrology time itself and the transfer time (also called "waiting time") has a significant impact on the total litho-metro cycle time. IM basically eliminates the transfer time and the metrology time from the total CT as IM sits in the cluster and measures within the shadow of the cluster's available time.

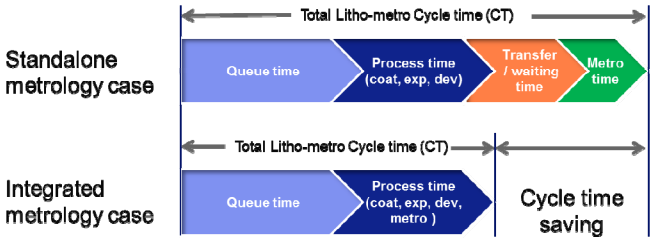


Figure 9. Total litho-metro cycle time

A significant number of lots (8000 lots with standalone vs. 11000 lots with IM at 20nm node HVM) are analyzed in litho-metro area in order to quantify the impact of integrated metrology in litho-metro cycle time. This measured data shows that a cycle time saving per layer of 28% (mean) and 46% (m+3s) of total litho-metro CT (overlay only) can be achieved with IM (compare to standalone metrology). For simplicity all the calculations done next use "mean" cycle time gain / layer.

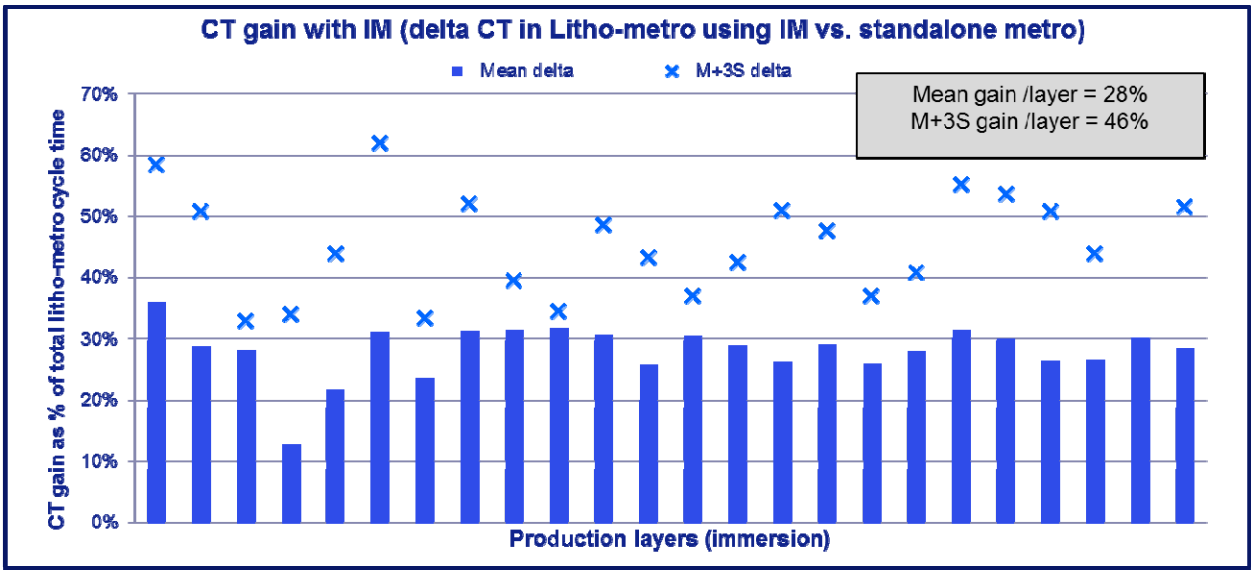


Figure 10. Cycle time benefit per immersion layer via integrated metrology (at 20nm node)

Using the above mentioned cycle time gain per layer measured at 20nm node; it is now possible to calculate the litho-metro cycle time gain at 1-x node. As mentioned in the previously discussed figure (figure 6), the number of metrology steps increase significantly from 20nm node to 1-x node. Cycle time also increases correspondingly.

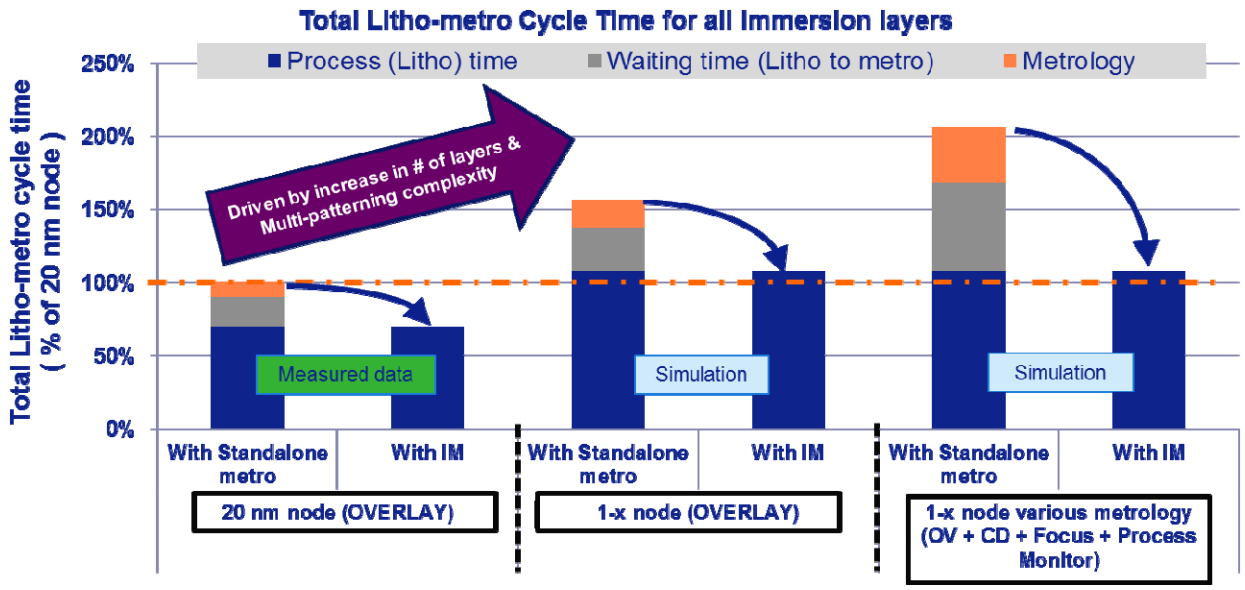


Figure 11. Reduction on average litho cluster cycle time with multi-layer target and integrated metrology

The figure above will quantify the benefit of a full implementation of multi-layer target and IM in 1-x node from total litho-metro cycle time point of view. Integration of 4 metrology applications (overlay, CD, focus, process monitoring) on IM (in the track) can cut cycle time in half at 1-x node.

There are several ways to quantify the impact of a decrease of cycle time in HVM. One of them is the reduction in WIP and another is the potential to increase scanner utilization. Calculation of WIP reduction shows that for immersion layers the above 28% of cycle time benefit of IM can translate into a WIP reduction per scanner of 1800 wafers (= CT benefit of all immersion layers * average scanner wph) and alternatively this can also translate into 2 to 5% increase potential in scanner utilization.

5. CONCLUSION

High volume implementation of diffraction-based overlay (μDBO with 16 μm x 16 μm targets) and integrated metrology are complete at 20nm node and ongoing at 1-x node. Metrology targets are designed with the goal of best accuracy via a simulation-based target design (Design-for-Control or "D4C"). Next, optimized metro-recipes of YieldStar μDBO are used to measure these targets to get the best on-product performance that is accurate and provides good precision and tool matching. Accuracy is demonstrated via good matching between YieldStar measurements on D4C generated μDBO targets (after develop) and CDSEM overlay measurement on device-like structures (after etch). It is also shown that tool matching (overlay) from 125 YieldStar tools in production meets the p2p matching (max delta overlay between two YieldStar tools) of 10% of the on-product overlay requirement.

The growing number of immersion layers and the need of multi-layer overlay measurement in process correction increase significantly in 1-x node driven by multi-patterning complexity, via-last process etc. These drive the cost of metrology higher (CAPEX and cycle time). If no action is taken, the total metrology time can increase by 80% at 1-x node compare to 20nm node. Multi-layer μDBO targets (designed by D4C) are introduced to enable measurement of multiple layers overlay in a single acquisition. With a proper implementation of the multi-layer target, the impact of metro time increase mentioned above can be reduced significantly. Actually, the # of metro tools per immersion metro pass can be reduced by almost 40% with the implementation of multi-layer overlay measurements in single acquisition on YieldStar.

However, the metrology time mentioned above is actually a small part of the total litho-metro cycle time and going from 20nm node to 1-x node this total cycle time increases by 60%. Measured data shows that transfer times from litho to metro (involved when standalone metrology is used) is actually much larger than the metrology time itself and the

transfer time (also called "waiting time") has a significant impact on the total litho-metro cycle time. A large amount of HVM data from 20nm node shows that a cycle time saving per layer of 28% (mean) and 46% (m+3s) of total litho-metro CT (overlay only) can be achieved with IM (compare to standalone metrology). Based on this measured data, it is possible to calculate that integration of 4 metrology applications (overlay, CD, focus, process monitoring) on IM (in the track) can cut cycle time in half at 1-x node.

It can be also calculated that this improvement in cycle time can translate to 1800 wafers WIP reduction in the fab per scanner and alternatively this results in 2 to 5% increase potential in scanner utilization.

Overall, an accurately designed multi-layer μDBO target (by D4C) provides a cost-effective solution for multi-layer overlay application on YieldStar while integrated metrology keeps the litho-metro cycle under control going from 20nm to 1-x node.

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